**ABSTRACT**

A memory system having a plurality of T-RAM cells arranged in an array is presented where each T-RAM cell has dual vertical devices and is fabricated over a SiC substrate. Each T-RAM cell has a vertical thyristor and a vertical transfer gate. The top surface of each thyristor is coplanar with the top surface of each transfer gate within the T-RAM array to provide a planar cell structure for the T-RAM array. A method is also presented for fabricating the T-RAM array having the vertical thyristors, the vertical transfer gates and the planar cell structure over the SiC substrate.